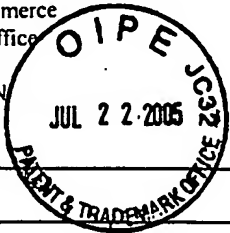


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<i>MX</i> ✓ <i>MX</i> ✓ <i>MX</i> ✓ <i>MX</i> ✓ <i>MX</i> ✓ <i>MX</i> ✓	Aragon, J.L., Gonzales, J., Gonzales, A., "Power-Aware Control Speculation Through Selective Throttling," Proceedings of the 9 th International Symposium on High-Performance Computer Architecture, February 2003. Balasubramonian, R., Albonesi, D.H., Buyuktosunoglu, A., Dwarkadas, S., "Memory Hierarchy Reconfiguration for Energy and Performance in General-Purpose Processor Architectures," 22 nd International Symposium on Microarchitecture, pp. 245-257, 2000. Barnes, R.D., Nystrom, E.M., Merten, M.C., Hwu, W.W., "Vacuum Packing: Extracting Hardware-Detected Program Phases for Post-Link Optimization," 35 th International Symposium on Microarchitecture, December 2002. Brooks, D., Martonosi, M., "Dynamic Thermal Management for High-Performance Microprocessors," In International Symposium on High-Performance Computer Architecture (HPCA-7), January 2001. Buyuktosunoglu, A., Karkhanis, T., Albonesi, D.H., Bose, P., "Energy Efficient Co-Adaptive Instruction Fetch and Issue," 30 th Annual International Symposium on Computer Architecture, June 2003. Dhodapkar, A., Smith, J.E., "Comparing Program Phase Detection Techniques," Proc. of the Int. Symposium on Microarchitecture, 2003.
Examiner <i>M. Muthuman</i>	Date Considered <i>7.18.2006</i>

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	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
MX	Dhodapkar, A.S., Smith, J.E., "Managing Multi-Configuration Hardware via Dynamic Working Set Analysis," 29 th International Symposium on Computer Architecture (ISCA 2002), Alaska, May 2002.						
MX	Dropsho, S., Buyuktosunoglu, A., Balasubramoniam, R., Albonesi, D.H., Dwarkadas, S., Semerar, G., Magklis, G., Scott, M.L., Integrating Adaptive On-Chip Storage Structures for Reduced Dynamic Power," International Conference on Parallel Architectures and Compilation Techniques, September 2002.						
MX	http://charlotte.ucsd.edu/~calder/simpoint/ , retrieved from the Internet June 3, 2005, pp. 1-2. 'Sim Point'						
MX	Huang, M., Renau, J., Torrelas, J., "Positional Adaptation of Processors: Application to Energy Reduction," In 30 th Annual International Symposium on Computer Architecture, June 2003.						
MX	Lafage, T., Seznec, A., "Choosing Representative Slices of Program Execution for Microarchitecture Simulations: A Preliminary Application to the Data Stream," In Workload Characterization of Emerging Applications, Kluwer Academic Publishers, September 2000, pp 149-163.						
Examiner M. Stehman				Date Considered 7.18.2006			
*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
	Merten, M.C., Trick, A.R., George, C.N., Gyllenhaal, J.C., Hwu, W.W., "A Hardware-Driven Profiling Scheme for Identifying Hot Spots to Support Runtime Optimization," 26 th International Symposium on Computer Architecture, pp. 136-147, May 1999.						
	Sherwood, T., Calder, T., "Time Varying Behavior of Programs," UCSD Technical Report, CS99-630, August 1999, pp. 1-16. http://www-cse.ucsd.edu/~calder/papers/UCSD-CS99-630.pdf						
	Sherwood, T., Perelman, E., Calder, B., "Basic Block Distribution Analysis to Find Periodic Behavior and Simulation Points in Applications," Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT 2001), Sept. 2001, Barcelona, Spain. http://www-cse.ucsd.edu/calder/papers/PACT-01-BBDA.pdf						
	Sherwood, T., Perelman, E., Hamerly, G., Calder, B., "Automatically Characterizing Large Scale Program Behavior," Proceedings of the 10 th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2002), October 2002, San Jose, California. http://www-cse.ucsd.edu/calder/papers/ASPLOS-02-SimPoint.pdf						
	Wunderlich, R., Wenisch, T., Falsafi, B., Hoe, J., "Smarts: Accelerating Microarchitecture Simulation Via Rigorous Statistical Sampling," In 30 th Annual International Symposium on Computer Architecture, June 2003.						
Examiner	M. Shults		Date Considered			7.18.2006	
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
my	Zhang, C., Vahid, F., Najjar, W., "A Highly-Configurable Cache Architecture for Embedded Systems," 30 th Annual International Symposium on Computer Architecture, June 2003.						
my	Hind, Michael J., Rajan, Vadakkedathu T., Sweeney, Peter F., "Phase Shift Detection: A Problem Classification," IBM Research Report, IBM T.J. Watson Research Center, Hawthorne, NY, August 4, 2003.						
my	Lau, Jeremy, Schoenmackers, Stefan, Calder, Brad, "Transition Phase Classification and Prediction," 11 th Int. Symposium on High Performance Computer Architecture, February 2005.						
my	Smith, James, E., Dhodapkar, Ashutosh, S., "Dynamic Microarchitecture Adaptation Via Co-Designed Virtual Machines," ISSCC 2002.						
my	Duesterwald, Evelyn, Cascaval, Calin, Dwarkadas, Sandhya, "Characterizing and Predicting Program Behavior and its Variability," Proc. of the 12 th Int. Conference on Parallel Architectures and Compilation Techniques, 2003.						
M. Stettin				7.18.2002			
*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							